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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,019	05/03/2001	Michael B. Raynham	10004324-1	5705

7590 01/04/2005

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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/848,019	RAYNHAM, MICHAEL B.	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13-23 and 27-30* is/are rejected.

7)☐ Claim(s) *9-12 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-7, 13-22 and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Bauman et al.

6. Bauman teaches the invention (claim 1) as claimed including a memory controller emulator for controlling memory devices in a memory system comprising:

a counter for generating a plurality of address values (e.g., see Figure 11); and,

a plurality of storage devices coupled to the counter for storing memory address information, memory data to be stored in the memory devices, and memory commands for controlling operation of the memory devices, each of the plurality of storage devices configured

to output data stored therein based upon address values received from the counter as the solid state memory modules (e.g., see Figure 1).

As to claim 2, Bauman teaches the memory controller emulator is a programmable logic device as part of the SMP environment (e.g., see col. 5, lines 15-62).

As to claim 3, Bauman teaches the storage devices are ROMs as being inherent as every system such as the one taught by the reference has read only memory which stores device drivers and the operating system as part of the memory system.

As to claim 4, Bauman teaches the memory commands, memory address information, memory data stored in the ROMs are programmable by a computer as being inherent as every system such as the one taught by the reference has read only memory which stores device drivers and the operating system as part of the memory system.

As to claim 5, Bauman teaches the memory data includes error correction code information (e.g., see col. 7, lines 24-42 and col. 11, lines 3-14).

As to claim 6, Bauman teaches the memory address information includes row address information, column address information and bank address information (e.g., see col. 4, lines 38-65).

As to claim 7, Bauman teaches the memory address information includes chip select information as part of the interconnections not specifically shown (e.g., see col. 5, line 47 to col. 6, line 24).

As to claim 13, Bauman teaches the plurality of address values include a start address and an end address and wherein the start address and the end address are programmable as programmable elements of the testing and initialization (e.g., see col. 4, line 37 to col. 5, line 22).

As to claim 14, Bauman teaches the memory data is stored in a first and a second storage device that each output memory data at a first output rate, the memory controller emulator further comprising:

a multiplexer for selectively outputting data from the first and the second storage devices (e.g., see Figure 10); and,

a register for receiving memory data output by the multiplexer, the register outputting the received memory data at a second output rate that is about double the output rate of the first output rate (e.g., see Figure 10).

As to claim 15, Bauman teaches a first and a second storage device each output strobe signals at a fist output rate, the memory controller emulator further comprising:

a multiplexer for selectively outputting strobe signals from the first and the second storage devices (e.g., see Figure 10); and,

a register for receiving strobe signals output by the multiplexer, the register outputting the received strobe signals at a second output rate that is about double the output rate of the first output rate (e.g., see Figure 10).

7. Bauman teaches the invention (claim 16) as claimed including a method of emulating a memory controller for controlling memory devices in a memory system comprising:

storing memory address information, memory data to be stored in the memory devices, and memory commands for controlling operation of the memory devices (e.g., see Figure 11);

automatically generating a plurality of sequential values (e.g., see Figure 11 and col. 21, line 59 to col. 22, line 63); and,

outputting stored memory address information, memory data and memory commands based upon the generated sequential values (e.g., see Figure 11 and col. 21, line 59 to col. 22, line 63).

As to claim 17, Bauman teaches the method is implemented using a programmable logic device as part of the SMP environment (e.g., see col. 5, lines 15-62).

As to claim 18, Bauman teaches the memory address information, memory data and memory commands are stored in at least one ROM of the programmable logic device as being inherent as every system such as the one taught by the reference has read only memory which stores device drivers and the operating system as part of the memory system.

As to claim 19, Bauman teaches inputting memory address information, memory data and memory commands into a computer and downloading the memory address information, memory data and memory commands to a programmable logic device as being inherent as every system such as the one taught by the reference has read only memory which stores device drivers and the operating system as part of the memory system.

As to claim 20, Bauman teaches the memory data includes error correction code information (e.g., see col. 7, lines 24-42 and col. 11, lines 3-14).

As to claim 21, Bauman teaches the memory address information includes row address information, column address information and bank address information (e.g., see col. 4, lines 38-65).

As to claim 22, Bauman teaches the memory address information includes chip select information as part of the interconnections not specifically shown (e.g., see col. 5, line 47 to col. 6, line 24).

As to claim 27, Bauman teaches the plurality of sequential values include a start value and an end value, wherein the start value and the end value are programmable (e.g., see Figure 11 and col. 21, line 59 to col. 22, line 63).

As to claim 28, Bauman teaches storing the memory data in odd and even banks, the odd and even banks each configured to output memory data at a first output rate and providing a register for receiving memory data output by the odd and even banks, the register configured to output the received memory data at a second output rate that is about double the output rate of the first output rate (e.g., see Figure 11 and col. 21, line 59 to col. 22, line 63).

As to claim 29, Bauman teaches storing strobe signals in odd and even banks, the odd and even banks each configured to output strobe signals at a first output rate and providing a register for receiving for strobe signals output by the odd and even banks, the register configured to output the received strobe signals at a second output rate that is about double the output rate of the first output rate (e.g., see Figure 11 and col. 21, line 59 to col. 22, line 63).

8. Bauman teaches the invention (claim 30) as claimed including a memory controller emulator comprising:

at least one storage device for storing signal information representing signals transmitted from a memory controller to a memory module (e.g., see Figure 11); and,

an address generator coupled to at least one storage device, the address generator configured to output address information, the storage device configured to output information based upon address information received from the address generator (e.g., see Figure 11).

9. Claims 9-12 and 24-26 read over the art of record but are objected to as being dependent upon a rejected base claim.

35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 8 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauman et al.

12. As to claims 8 and 23, Bauman teaches the limitations of the claim dependency, however, the reference does not specifically teach basics specific to actual testing. It would have been obvious to one of ordinary skill in the art at the time the invention was made to store scope synchronization information to be output to an oscilloscope because an oscilloscope is to be used for specific electrical connection tests.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

December 22, 2004